CLAIMS:

1. A circuit testing system, for testing a circuit under test (24) with logic circuits (12) and a scan chain comprising flip-flop cells (10a-c) with inputs and outputs operationally connected to the logic circuits (12), the circuit under test (24) comprising a plurality of clock domains, each containing a respective part of the flip-flop cells (10a-c) at are clocked by a respective domain clock signal, (CLKa, CLKb, CLKc) the circuit testing system comprising:

- a test controller (22) arranged to switch the circuit under test (24) to a test mode wherein the test controller (22) supplies successive test input patterns through the scan chain (10a-c), each test input pattern being associated with a respective combination of domain clock signals that are selectively enabled to capture a response of the logic circuits (12) to the test input pattern into flip-flop cells (10a-c) of the scan chain, the test controller (22) using the captured response from at least part of the flip-flop cells (10a-c) to detect faults in the circuit under test (24);

- a test pattern selector (20) arranged to select a set of test input patterns and the associated combinations of domain clock signals for use by the test controller (22), wherein a particular test pattern in the selected set that has the properties that:

- the response to the particular test pattern captured by a timing sensitive flip-flop cell (10a-c) in a first clock domain is used to detect a fault,

- the timing sensitive flip-flop cell (10a-c) receives data dependent on data from a source flip-flop cell (10a-c) that belongs to a second clock domain different from the first clock domain,

- the combination of selectively enabled domain clock signals associated with the particular test pattern comprises the clocks of both the first and second domain,

also has the further property that the data value in the source flip-flop cell (10a-c) is identical to a response value captured by the source flip-flop cell (10a-c) for the particular test pattern.

2. A circuit testing system according to claim 1, wherein the test pattern selector (22):

- stores information representing an original design that corresponds to the circuit under test (24);
- includes, with each test pattern, clock status signals that indicate whether respective ones of the domain clocks (CLKa, CLKb, CLKc) must be disabled during capture of a response to the test pattern;
- generates an adapted version of the original design, wherein additional logic circuits (30, 40, 42) have been added to the original design, the additional logic circuits (30, 40, 42) being designed to selectively enable a dependence of an input signal of the timing sensitive flip-flop cell (10a-c) on data from the source flip-flop (10a-c) according to the original design, when the clock status signals indicate that the second domain clock is disabled, the additional circuits also enabling the dependence when the input and output signals of the source flip-flop cell (10a-c) are identical and the second domain clock is enabled;
- uses the adapted version to select the test patterns with associated clock status signals so that a set of logic circuit faults is covered for the adapted version.

3. A method of testing a circuit under test (24) with logic circuits (12) and a scan chain comprising flip-flop cells (10a-c) with inputs and outputs operationally connected to the logic circuits (12), the circuit under test comprising a plurality of clock domains, each containing a respective part of the flip-flop cells (10a-c) that are clocked by a respective domain clock signal(CLKa, CLKb, CLKc); the method comprising:
- selecting a set of test input patterns each with an associated combination of domain clock signals that will be selectively enabled to capture a response to the test pattern, wherein the set contains a particular test pattern that has the properties that:
  - the response to the particular test pattern captured by a timing sensitive flip-flop cell (10a-c) in a first clock domain is used to detect a fault,
  - the timing sensitive flip-flop cell (10a-c) receives data dependent on data from a source flip-flop cell (10a-c) that belongs to a second clock domain different from the first clock domain,
  - the combination of selectively enabled domain clock signals associated with the particular test pattern comprises the clocks of both the first and second domain,
- the particular test pattern also having the further property that the data value in the source flip-flop cell (10a-c) is identical to a response value captured by the source flip-flop cell (10a-c) for the particular test pattern;

- switching the circuit under test (24) to a test mode,
- supplying successive test input patterns from said set through the scan chain, including the particular test pattern;
- selectively enabling the combination of domain clock signals associated with each test pattern to capture a response of the logic circuits to the test pattern into flip-flop cells (10a-c) of the scan chain,
- using the captured response from at least part of the flip-flop cells to detect faults in the circuit under test (24), including the response captured by the timing sensitive flip-flop cell (10a-c) in response to the particular test pattern.

4. A method of testing according to claim 3, wherein the step of selecting the set of test patterns comprises:
- receiving information representing an original design that corresponds to the circuit under test (24);
- including with each pattern clock status signals that indicate whether respective ones of the domain clocks will be disabled during capture of a response to the pattern;
- generating an adapted version of the original design wherein additional logic circuits (30, 40, 42) have been added to the original design, the additional logic circuits (30, 40, 42) being designed to selectively enable a dependence of an input signal of the timing sensitive flip-flop cell (10a-c) on data from the source flip-flop cell (10a-c) according to the original design, when the clock status signals indicate that the second domain clock is disabled, the additional circuits (30, 40, 42) also being designed to enable the dependence when the input and output signals of the source flip-flop cell (10a-c) are identical and the second domain clock is enabled;
- selecting the set of test patterns with associated clock status signals for the adapted version so that a set of logic circuit faults is covered for the adapted version.

5. A method of testing according to claim 4, comprising:
- tracing back from the input of the timing sensitive flip-flop cell (10a-c) through the logic circuits (12) in the original design until a circuit node is encountered at which node signals depend on the data from the source flip-flop cell (10a-c) but not on any data from flip-flop cells (10a-c) outside the first and second clock domain;

- said generating including adding an additional gate in the adapted version of the design at said circuit node to realize said selectively enabled dependence.

6. A medium carrying a set of test patterns for testing a circuit under test (24) with logic circuits (12) and a scan chain comprising flip-flop cells (10a-c) with inputs and outputs operationally connected to the logic circuits (12), the circuit under test comprising a plurality of clock domains, each containing a respective part of the flip-flop cells (10a-c) that are clocked by a respective domain clock signal(CLKa, CLKb, CLKc); each of the set of test input patterns being associated with an associated combination of domain clock signals that will be selectively enabled to capture a response to the test pattern, wherein the set contains a particular test pattern that has the properties that:

- the response to the particular test pattern captured by a timing sensitive flip-flop cell (10a-c) in a first clock domain is used to detect a fault,
- the timing sensitive flip-flop cell (10a-c) receives data dependent on data from a source flip-flop cell (10a-c) that belongs to a second clock domain different from the first clock domain,
- the combination of selectively enabled domain clock signals associated with the particular test pattern comprises the clocks of both the first and second domain,
- the particular test pattern also having the further property that the data value in the source flip-flop cell (10a-c) is identical to a response value captured by the source flip-flop cell (10a-c) for the particular test pattern.

7. A method of generating a set of test patterns for a circuit under test (24) with logic circuits (12) and a scan chain comprising flip-flop cells (10a-c) with inputs and outputs operationally connected to the logic circuits (12), the circuit under test comprising a plurality of clock domains, each containing a respective part of the flip-flop cells (10a-c) that are clocked by a respective domain clock signal(CLKa, CLKb, CLKc); each test pattern being an associated combination of domain clock signals that will be selectively enabled to capture a response to the test pattern, the method comprising:

- receiving information representing an original design that corresponds to the circuit under test (24);
- including with each pattern clock status signals that indicate whether respective ones of the domain clocks will be disabled during capture of a response to the pattern;

- generating an adapted version of the original design wherein additional logic circuits (30, 40, 42) have been added to the original design, the additional logic circuits (30, 40, 42) being designed to selectively enable a dependence of an input signal of the timing sensitive flip-flop cell (10a-c) on data from the source flip-flop cell (10a-c) according to the original design, when the clock status signals indicate that the second domain clock is disabled, the additional circuits (30, 40, 42) also being designed to enable the dependence when the input and output signals of the source flip-flop cell (10a-c) are identical and the second domain clock is enabled;
- selecting the set of test patterns with associated clock status signals for the adapted version so that a set of logic circuit faults is covered for the adapted version.

8. A method generating a set of test patterns according to claim 7, the method comprising:
- tracing back from the input of the timing sensitive flip-flop cell (10a-c) through the logic circuits (12) in the original design until a circuit node is encountered at which node signals depend on the data from the source flip-flop cell (10a-c) but not on any data from flip-flop cells (10a-c) outside the first and second clock domain;
- said generating including adding an additional gate in the adapted version of the design at said circuit node to realize said selectively enabled dependence.

9. A test pattern generating machine for generating a set of test patterns for a circuit under test (24) with logic circuits (12) and a scan chain comprising flip-flop cells (10a-c) with inputs and outputs operationally connected to the logic circuits (12), the circuit under test comprising a plurality of clock domains, each containing a respective part of the flip-flop cells (10a-c) that are clocked by a respective domain clock signal(CLKa, CLKb, CLKc); each test pattern being an associated combination of domain clock signals that will be selectively enabled to capture a response to the test pattern, the machine being arranged to:
- receive information representing an original design that corresponds to the circuit under test (24);
- include with each pattern clock status signals that indicate whether respective ones of the domain clocks will be disabled during capture of a response to the pattern;
- generating an adapted version of the original design wherein additional logic circuits (30, 40, 42) have been added to the original design, the additional logic circuits (30, 40, 42) being designed to selectively enable a dependence of an input signal of the timing

sensitive flip-flop cell (10a-c) on data from the source flip-flop cell (10a-c) according to the original design, when the clock status signals indicate that the second domain clock is disabled, the additional circuits (30, 40, 42) also being designed to enable the dependence when the input and output signals of the source flip-flop cell (10a-c) are identical and the second domain clock is enabled;

- selecting the set of test patterns with associated clock status signals for the adapted version so that a set of logic circuit faults is covered for the adapted version.

10. A computer program product containing machine instructions for generating a set of test patterns for a circuit under test (24) with logic circuits (12) and a scan chain comprising flip-flop cells (10a-c) with inputs and outputs operationally connected to the logic circuits (12), the circuit under test comprising a plurality of clock domains, each containing a respective part of the flip-flop cells (10a-c) that are clocked by a respective domain clock signal(CLKa, CLKb, CLKc); each test pattern being an associated combination of domain clock signals that will be selectively enabled to capture a response to the test pattern, the instructions being arranged to:

- receive information representing an original design that corresponds to the circuit under test (24);
- include with each pattern clock status signals that indicate whether respective ones of the domain clocks will be disabled during capture of a response to the pattern;
- generating an adapted version of the original design wherein additional logic circuits (30, 40, 42) have been added to the original design, the additional logic circuits (30, 40, 42) being designed to selectively enable a dependence of an input signal of the timing sensitive flip-flop cell (10a-c) on data from the source flip-flop cell (10a-c) according to the original design, when the clock status signals indicate that the second domain clock is disabled, the additional circuits (30, 40, 42) also being designed to enable the dependence when the input and output signals of the source flip-flop cell (10a-c) are identical and the second domain clock is enabled;
- selecting the set of test patterns with associated clock status signals for the adapted version so that a set of logic circuit faults is covered for the adapted version.